UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,146	09/24/2003	Mei Luo	A1070	7382

45851 7590 01/11/2005

G. VICTOR TREYZ
FLOOD BUILDING
870 MARKET STREET, SUITE 984
SAN FRANCISCO, CA 94102

EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,146	LUO ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-10 and 19-36* is/are allowed.

6)☒ Claim(s) *1-4,11,13-16,18,27 and 29-32* is/are rejected.

7)☒ Claim(s) *5,12,17,28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the submitted drawings of 9/24/03 are not formal drawings. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 11, 13-16, 18, 27 and 29-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Gabara (U. S. PAT. 5,977,796).

In claim 1, Gabara teaches all claimed features in Fig. 2, dynamically adjustable differential output driver circuitry on an integrated circuit (chip 1) that transmits differential output data signals (24, 26) that have a peak-to-peak output voltage swing (col. 4, line 8) V_{OD}, comprising: adjustable current source circuitry (20, 22); adjustable resistor circuitry (18'); switching circuitry (A1, B2, B1, A2) for switching current from the adjustable current source circuitry through the adjustable resistor circuitry (18') to produce the differential output signals, wherein the adjustable current source circuitry

and adjustable resistor circuitry are controlled independently (20, 22 controlled by V_{source}, V_{sink} ; and wherein 18' controlled by a voltage control, col. 3, line 46) in real time by control signals to adjust the peak-to-peak output voltage swing V_{OD} of the differential output data signals.

In claim 2, Gabara further teaches in Fig. 6, the dynamically adjustable differential output driver circuitry defined in claim 1 further comprising an adjustable voltage source (101), wherein the differential output data signals have a common-mode voltage Vcm that is controlled by adjusting the adjustable voltage source (col. 9, lines 30-45).

In claim 3, Gabara further teaches in Fig. 2, the dynamically adjustable differential output driver circuitry defined in claim 1 further comprising dynamic control circuitry (45) that generates the control signals that control the adjustable current source circuitry and the adjustable resistor circuitry.

In claim 4, Gabara further teaches in Fig. 6, the dynamically adjustable differential output driver circuitry defined in claim 1 further comprising dynamic control circuitry (not shown) that generates control signals (V_{res})that control the adjustable voltage source (101).

In claim 11, Gabara teaches all claimed features in Fig. 2, an integrated circuit, comprising: a dynamically adjustable differential output driver (11) that produces differential output data signals having a peak-to-peak output voltage swing (col. 4, line 8) V_{OD}; and dynamic control circuitry (45) that receives information (V_{low}, V_{high}) from another integrated circuit (Chip 2) to which the differential output data signals are

transmitted and which controls the dynamically adjustable differential output driver dynamically (V_{source}, V_{sink}) in real time to adjust the peak-to-peak output voltage swing V_{OD} based at least partly on the information received from the other integrated circuit.

In claim 13, Gabara further teaches in Fig. 2, the integrated circuit defined in claim 11 wherein the dynamically adjustable differential output driver comprises adjustable current source circuitry (20, 22) and wherein the dynamic control circuitry adjusts the peak-to-peak output voltage swing V_{OD} by adjusting the adjustable current source circuitry.

In claim 14, Gabara further teaches in Figs. 2 and 6, the integrated circuit defined in claim 11 wherein the dynamically adjustable differential output driver comprises adjustable resistor circuitry (18') and wherein the dynamic control circuitry adjusts the peak-to-peak output voltage swing V_{OD} by adjusting the adjustable resistor circuitry.

In claim 15, Gabara further teaches in Fig. 2, the integrated circuit defined in claim 11 wherein the dynamically adjustable differential driver comprises adjustable current source output circuitry (20, 22); the dynamic control circuitry (45) adjusts the peak-to-peak output voltage swing V_{OD} by adjusting the adjustable current source circuitry; the dynamically adjustable differential output driver comprises adjustable resistor circuitry (18'); the dynamic control circuitry adjusts the peak-to-peak output voltage swing V_{OD} by adjusting the adjustable resistor circuitry; and the dynamic control circuitry adjusts the adjustable current source circuitry (V_{source}, V_{sink}) independently from the adjustable resistor circuitry (a voltage control, col. 3, line 46).

In claim 16, Gabara further teaches in Figs. 2 and 6, the integrated circuit defined in claim 11 wherein the differential output data signals have a common-mode voltage Vcm (col. 9, lines 30-45) and wherein the dynamically adjustable differential output driver comprises an adjustable voltage source (101) that the dynamic control circuitry adjusts based at least partly on the information received from the other integrated circuit to control the common-mode voltage Vcm of the differential output data signals.

In claim 18, Gabara further teaches in Figs. 2 and 6, the integrated circuit defined claim 11 wherein the differential output data signals (24, 26) have a common-mode voltage when transmitted from the integrated circuit (11) to a differential input driver (12') on the other integrated circuit, wherein the differential input driver has a common-mode voltage level (inherency), wherein the information received from the other integrated circuit comprises information on the common-mode voltage level of the differential input driver, and wherein the dynamically adjustable differential output driver (11) comprises an adjustable voltage source (101) that the dynamic control circuitry adjusts to match the common-mode voltage of the differential output data signals to the common-mode voltage level of the differential input driver.

Method claims 27 and 29-32 correspond to detailed circuitry already discussed similarly with regard to claims 11, 13-16 and 18.

4. Claims 5, 12, 17 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 6-10 and 19-36 appear to comprise allowable subject matters.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER

Vibol Tan

Primary Examiner, AU 2819